2186

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Date: May 27, 2005 Name: Joseph F. Hetz, Esq. Signature: _____

BRINKS HOFER GILSON & LIONE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Appln. of:	Moore et al.	
Appln. No.:	09/877,720	Examiner: Z. Li
Filed:	June 8, 2001	Art Unit: 2186
For:	Memory Device and Method for Storing and Reading a File System Structure in a Write-Once Memory Array	
Attorney Docket No:	10519-32	

Mail Stop Amendment
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Respectfully submitted,

Joseph F. Hetz, Esq. (Reg. No. 41,070)

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Joseph F. Hetz - Reg. No. 41,070
Name of Applicant, Assignee or Registered Representative

Signature

Our Case No. 10519-32

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Moore et al.	Examiner:	Z. Li
Serial No.:	09/877,720	Group Art Unit:	2186
Filed:	June 8, 2001		
For:	Memory Device and Method for Storing and Reading Data in a Write-Once Memory Array		

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

This Appeal is in response to the Final Office Action mailed November 5, 2004.

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I. Real Party in Interest

Matrix Semiconductor, Inc. is the real party in interest.

II. Related Appeals and Interferences

The appeal in U.S. patent application serial number 09/877,719, filed June 8, 2001, may directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.[1]

III. Status of Claims

Claims 1-21 are pending, stand rejected, and are the subject of this appeal.

IV. Status of Amendments

No amendments were filed subsequent to the final rejection.

V. Summary of Claimed Subject Matter

Applicants have invented a memory device and method for storing and reading data in a write-once memory array. In one disclosed method, which is claimed in Claim 1, a plurality of bits representing data to be stored in a write-once memory array are inverted. The inversion takes place irrespective of the number of logic one bits in the plurality of bits. Next, the inverted plurality of bits are stored in the write-once memory array. The inverted plurality of bits are later read from the write-once memory array, and the read inverted plurality of bits are inverted to return the bits to their pre-inverted form.

As described at pages 11-14 in Applicants' specification, this method finds particular advantage when a data storage device and/or a data reading device requires one or more 0s

[1] Applicants note that there is presently a non-final Office Action directed against U.S. patent application serial number 09/877,691, filed June 8, 2001. If differences with the Examiner cannot be resolved, Applicants may file an appeal in that application, and such an appeal may directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

before, between, or after stored data. For example, a string of 0s can represent the end of a file or can represent unallocated memory cells in the middle of a file. If Logic 0 is the initial, un-programmed digital state of a memory cell in a memory array,[2] additional data can later be written into these "empty" memory cells. However, if Logic 1 is the initial, un-programmed digital state, "empty" memory cells are created by switching the initial Logic 1 state to Logic 0, and those memory cells cannot later be switched back to 1s to store additional data. This problem is also encountered when memory cells have Logic 0 as their initial digital state and "empty" memory cells are designated as Logic 1. Accordingly, additional memory space must be used to store additional data.

The memory array of Figures 16A and 16B in Applicants' specification provides an illustration of this problem. In Figure 16A, data is stored at address 1 and 3. A string of 0s is stored at address 2 to represent unallocated memory cells in the middle of the file, and a string of 0s is stored at address 4 and 5 to represent the end of the file. If Logic 0 were the initial, un-programmed digital state of the memory array, additional data could be stored in the "empty" memory cells at address 2, 4, and 5. However, because these memory cells are permanently switched to a programmed Logic 0 state, additional data cannot be written into these memory cells and must be stored in another location of the memory array. As shown in Figure 16B, additional data is stored at address 6, 7, and 8 instead of address 2, 4, and 5.

With the method described above, the "empty" memory cells can be used to store additional data. Because bits representing data are inverted before they are stored in the memory array, all Logic 1 bits are stored as Logic 0 bits, and all Logic 0 bits are stored as Logic 1 bits.

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[2] The initial, un-programmed digital state can either be Logic 1 or 0, with the alternative, programmed digital state being Logic 0 or 1, respectively (see Claims 13 and 14).

Because Logic 1 is the initial state of the memory array, Logic 1 bits are "stored" by not switching the initial state of a memory cell to Logic 0. Accordingly, some or all of these memory cells can later be switched to the Logic 0 state to store additional data in the "empty" cells. Figures 17A and 17B illustrate how this approach can be used with the previous example. As shown in Figure 17A, the data bits are inverted and stored as inverted data, and the 0s representing "empty" memory cells are inverted and stored as 1s. Since the initial digital state of the memory cells is Logic 1, the "empty" memory cells are left in the un-programmed state. Accordingly, some or all of these memory cells can later be programmed as 0s to store additional data (in an inverted form), as shown in Figure 17B.

In this disclosed embodiment, all data bits read from and stored in the memory array are inverted. That is, the data bits are inverted irrespective of a number of logic one bits in the plurality of bits (see, for example, Figures 16A and 17A, which show that the data string 0000 is inverted even though the number of logic one bits (zero) does not exceed fifty percent of the total number of bits (four)). By inverting data bits irrespective of the number of logic one bits in the plurality of bits to be inverted, this method essentially redefines the initial, un-programmed digital state of the memory cells as the alternative, programmed digital state (see Claims 12 and 19-21). In the example above, the initial, un-programmed digital state is redefined as Logic 0, which allows memory space to be conserved by storing additional data in "empty" memory cells instead of using additional memory cells. In this way, the memory cells at address 6, 7, and 8 are not wasted by storing additional data that could be stored in the "empty" memory cells at address 2, 4, and 5. When data bits are read from the memory array, they are inverted to provide the data bits in their original, non-inverted configuration.

Hardware and/or software in a data storage device, data reading device, and/or write-once memory device can be responsible for inverting data bits to be stored in or read from a write-once memory array. Figures 18-21 illustrate various configurations. In Figure 18, the data storage device 600 is responsible for inverting data bits to be stored in the memory array 620 (see Claim 2). In Figure 19, a controller 615 in the memory device 610 is responsible for inverting inverted data bits read from the memory array 620 (see Claims 7 and 8). In Figure 20, a controller 715 in the memory device 710 is responsible for inverting data bits to be stored in the memory array 720 (see Claims 4 and 9). In Figure 21, the data reading device 840 is responsible for inverting data bits read from the memory array 820 (see Claim 5).

The data storage device and/or the data reading device can be a digital audio player, a digital audio book, an electronic book, a digital camera, a game player, a general-purpose computer, a personal digital assistant, a portable telephone, a printer, or a projector (see Claims 3 and 6). The memory device can be a solid-state memory device (Claim 10) or an optical memory device (Claim 11) and can take the form of a two-dimensional (Claims 16 and 18) or three-dimensional (Claims 15 and 17) memory array.

VI. Grounds of Rejections to Be Reviewed on Appeal

Claims 1-21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the proposed combination of Vining et al.[3] in view of de la Iglesai et al.[4] and Ohno et al.[5]

[3] U.S. Patent No. 6,377,526.
[4] U.S. Patent No. 6,490,703.
[5] U.S. Patent No. 5,247,494.

VII. Argument

Applicants respectfully submit that the rejections of Claims 1-21 under 35 U.S.C. § 103(a) over the proposed combination of Vining et al., de la Iglesai et al., and Ohno et al. should be removed for the reasons set forth below.

A. Independent Claims 1 and 8

Independent Claims 1 and 8 each recite elements relating to inverting a plurality of bits irrespective of a number of logic one bits in the plurality of bits.[6] These claims were rejected as being obvious over the proposed combination of Vining et al., de la Iglesia et al., and Ohno et al. In the Office Action, the Examiner admitted that the combination of Vining et al. and de la Iglesia et al. does not show these elements and relied on Ohno et al. to cure this deficiency. Applicants respectfully submit that one skilled in the art would not have been motivated to combine Ohno et al. with Vining et al. and de la Iglesia et al., as proposed in the Office Action.

1. One Skilled in the Art Would Not Have Been Motivated to Combine Ohno et al. with Vining et al. and de la Iglesia et al.

Ohno et al. is directed to a specialized optical disk having a write-once zone and a re-writable zone, with each zone having a different chemical makeup. Because of the differences in chemical makeup, different techniques are used to record a "1" in each of the two zones. Specifically, to record a "1" in the write-once zone, a pulsed light beam is used to create a spot of ***high*** reflectance. In contrast, to record a "1" in the re-writable zone, a pulsed light beam is used to create a spot of ***low*** reflectance. Accordingly, a "1" is represented by a high reflectance spot in

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[6] Claim 1: "(a) inverting a plurality of bits representing data to be stored in a write-once memory array irrespective of a number of logic one bits in the plurality of bits"

Claim 8: "a controller . . . operative to invert the plurality of bits representing the data irrespective of a number of logic one bits in the plurality of bits"

the write-once zone and a low reflectance spot in the re-writable zone. Col. 9, lines 7-16 of Ohno et al. teach that it is desirable to make a "1" be represented by the same level of reflectance (low reflectance) across the entire disk, irrespective of whether the "1" is stored in the write-once zone or the re-writable zone. To accomplish this, Ohno et al. uses an inverter to cause a "1" to be recorded as a "0" in the write-once zone. In this way, an inverted "1" is stored as a spot of ***low*** reflectance instead of ***high*** reflectance, thereby providing the disk-wide consistency that Ohno et al. desires.

In the Office Action, it was asserted that one skilled in the art would have been motivated to add Ohno et al. to Vining et al. and de la Iglesia et al. "because it enables storage [of] data for a long time without necessitating use of a complicated configuration" of having a "1" being represented in different regions of an optical disk by spots of different levels of reflectance. Applicants respectfully submit that this is insufficient motivation to combine the references. As a first matter, the "complicated configuration" of having a "1" being represented by different levels of reflectance in different regions of an optical disk is not a problem in either Vining et al. or de la Iglesia et al. Vining et al. does not use the specialized "two-zone" optical disk disclosed in Ohno et al. with its spots of different levels of reflectance to store data, and de la Iglesia et al. is directed to semiconductor memory devices, which do not use reflectance to store data. Accordingly, neither Vining et al. nor de la Iglesia et al. presents the problem for which inverting is a solution. Simply put, one skilled in the art would not have been motivated to adopt a solution for a problem that does not exist.

Lack of motivation is further shown by the fact that the addition of Ohno et al. would be contrary to the basic operating principle of de la Iglesia et al. De la Iglesia et al. is directed to a bus power savings technique in which bits in a data string are inverted when the number of logic

one bits in the data string exceeds fifty percent of the total number of bits. This technique is described, *inter alia*, at col. 2, line 65 – col. 3, line 2 (emphasis added):

> In a preferred embodiment, the invention saves power in systems where power consumption is high during a logic one state by inverting the data signal ***when the number of bits at the logic one state in that data signal exceed [sic] fifty percent of the total number of bits***.

Because storing logic one bits requires more power that storing logic zero bits, inverting the bits when the majority of bits are logic one bits saves power. When the minority of bits are logic one bits, the bits are not inverted, since inverting the bits in that situation would result in more logic one bits and, hence, higher power consumption. Accordingly, the basic operating principle of de la Iglesia et al. is to save bus power by inverting bits in a data string when the number of logic one bits exceeds fifty percent of the total number of bits.

If de la Iglesia et al. were modified such that a data string is inverted irrespective of the number of logic one bits, some data strings would be stored with more logic one bits than logic zero bits. This would result in higher power consumption, thereby reintroducing the very problem that de la Iglesia et al. seeks to overcome.

In summary, Applicants respectfully submit that one skilled in the art would not have been motivated to combine Ohno et al. with Vining et al. and de la Iglesia et al. because Vining et al. and de la Iglesia et al. do not present the need for the solution set forth in Ohno et al. and because the addition of Ohno et al. would be contrary to the basic operating principle of de la Iglesia et al. Without the required motivation, the rejections are merely the result of using the claims as a blueprint to pick and choose isolated teachings from the prior art. Accordingly, Applicants respectfully request that the rejections of independent Claims 1 and 8 be withdrawn.

2. Comments on Examiner's "Response to Arguments"

In the "Response to Arguments" section of the Advisory Action, the Examiner paraphrases two sentences (col. 4, lines 24-27 and col. 9, lines 19-23) from Ohno et al. and offers those sentences as motivation to combine Ohno et al. with Vining et al. and de la Iglesia et al.:

> to enhance the usefulness of [an] optical disk without necessitating the use of complicated head configuration and complicated head control system for recording, reproducing, and erasing, so that the output data from the computer can be easily edited and filed, thereby enabling storage of a long time by utilizing only one optical disk

Applicants respectfully submit that these sentences do not provide the required motivation. As a first matter, there is no proffered nexus between the quoted language in Ohno et al. and Vining et al. and de la Iglesia et al. Something more than a bald quote from one reference is needed to show motivation to combine that reference with another reference. The motivation requirement would be meaningless if motivation could be shown merely by quoting from one reference because such "motivation" could be used to combine any two references without regard to the teaching of the references.

As a second matter, the passages in Ohno et al. that precede the quoted sentences make clear that the cited advantages are achieved with the specialized "two-zone" optical disk disclosed in Ohno et al. (see, for example, col. 3, lines 64 – col. 4, line 23). Accordingly, contrary to the Examiner's assertion, the proposed combination ***does*** require the use of the specialized "two-zone" optical disk disclosed in Ohno et al. since it is necessary to achieve the purpose cited by the Examiner as providing motivation to combine the references. Since the proposed combination requires the use of the specialized "two-zone" ***optical*** disk and de la Iglesia et al. is directed to a ***solid state*** device, Applicants respectfully submit that Ohno et al. and

de la Iglesia et al. cannot be combined, as de la Iglesia et al. teaches away from the memory device required by Ohno et al.

Lastly, as further evidence of motivation, the Examiner cited boilerplate language in Vining et al. and de la Iglesia et al. that "the present invention may be embodied in other specific forms" and "the principle of the invention may be applied toward a wide range of systems." This boilerplate language is present in virtually every issued patent and provides no specific motivation for combining one reference with another. Indeed, if such language were sufficient to show motivation to combine, virtually every issued patent could be modified at will to render obvious any claimed invention.

B. Independent Claim 12

Independent Claim 12 recites "redefining the initial, un-programmed digital state of the plurality of write-once memory cells as the alternative, programmed digital state by storing bits in the plurality of write-once memory cells in an inverted form irrespective of a number of logic one bits in the plurality of bits." Like independent Claims 1 and 8, independent Claim 12 recites an element relating to inverting a plurality of bits irrespective of a number of logic one bits in the plurality of bits: "storing bits in the plurality of write-once memory cells in an inverted form irrespective of a number of logic one bits in the plurality of bits." Accordingly, Applicants respectfully submit that the rejection of independent Claim 12 should be removed for the same reasons set forth above with respect to independent Claims 1 and 8 (i.e., because there is no suggestion to combine Ohno et al. with Vining et al. and de la Iglesia et al.).

Additionally, even if Ohno et al. were combined with Vining et al. and de la Iglesia et al., the proposed combination would not yield each and every element recited in independent Claim 12. Independent Claim 12 requires that the initial, un-programmed digital state of write-once

memory cells of a write-once memory array be redefined as the alternative, programmed digital state by inverting stored bits. In order for the initial, un-programmed digital state of the memory array to be redefined, Logic 1 must be Logic 0, and vice versa, in all locations of the memory array; otherwise, there would not be a redefinition. With the proposed combination, the initial, un-programmed digital state of the memory array is not redefined because bits are not inverted in all locations of the memory array. Under the proposed combination, bits in one area of the memory array would be inverted, but bits in the other area would not. Because of this non-uniformity, a Logic 1 in some areas is really a Logic 1, while, in other areas, it is a Logic 0. Accordingly, the inversion in the proposed combination does not redefine the initial, un-programmed digital state as the alternative, programmed digital state, as recited in Claim 12.

C. Dependent Claims 2-7, 9-11, and 13-21

Dependent Claims 2-7, 9-11, and 13-21 depend from independent Claims 1, 8, and 12. Accordingly, these claims are patentable over the proposed combination for the reasons set forth above with respect to the independent claims. These dependent claims also provide an additional ground of patentability. The following describes some of those additional grounds.

1. Dependent Claim 10

Dependent Claim 10 recites that the memory device comprises a solid-state memory device. As described above, the motivation cited by the Examiner for combining Ohno et al. with Vining et al. and de la Iglesai et al. requires that an optical disk be used. Accordingly, the proposed combination does not yield a solid-state memory device.

2. Dependent Claims 15 and 17

Dependent Claims 15 and 17 recite that the write-once memory array comprises a three-dimensional memory array. The proposed combination does not teach a three-dimensional memory array. In Ohno et al. and Vining et al., the memory device is an optical disc, and in de la Iglesia et al., the memory device is a conventional two-dimensional memory array. Accordingly, even if it were proper to combine Vining et al., de la Iglesai et al., and Ohno et al., the proposed combination would not yield the elements recited in dependent Claims 15 and 17.

3. Dependent Claims 19-21

Dependent Claims 19-21 recite that the plurality of bits are inverted even when a number of logic one bits in the plurality of bits does not exceed fifty percent of a total number of bits in the plurality of bits. De la Iglesia et al. specifically teaches away from this element at col. 2, line 65 – col. 3, line 2 (emphasis added):

> In a preferred embodiment, the invention saves power in systems where power consumption is high during a logic one state by inverting the data signal ***when the number of bits at the logic one state in that data signal exceed [sic] fifty percent of the total number of bits***.

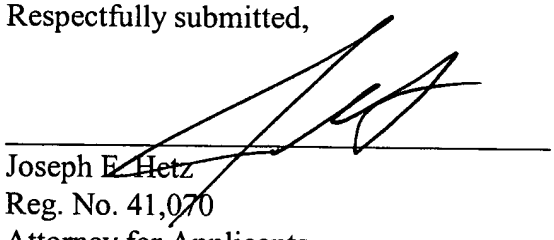
Because de la Iglesia et al. specifically teaches away from the element claimed in dependent Claims 19-21, Applicants respectfully submit that there is no motivation to make the combination proposed in the Office Action.

VIII. Conclusion

For the reasons set forth above, Applicants respectfully submit that Claims 1-21 are patentable over the proposed combination of Vining et al., de la Iglesai et al., and Ohno et al. Accordingly, Applicants respectfully request removal of the 35 U.S.C. § 103(a) rejections of Claims 1-21.

Dated: May 27, 2005

Respectfully submitted,



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IX. Claims Appendix

1. A method for storing and reading data in a write-once memory array, the method comprising:

(a) inverting a plurality of bits representing data to be stored in a write-once memory array irrespective of a number of logic one bits in the plurality of bits;

(b) storing the inverted plurality of bits in the write-once memory array;

(c) reading the inverted plurality of bits from the write-once memory array; and

(d) inverting the inverted plurality of bits read from the write-once memory array.

2. The method of Claim 1, wherein act (a) is performed by a data storage device coupled with a memory device comprising the write-once memory array.

3. The method of Claim 2, wherein the data storage device comprises a device selected from the group consisting of a digital audio player, a digital audio book, an electronic book, a digital camera, a game player, a general-purpose computer, a personal digital assistant, a portable telephone, a printer, and a projector.

4. The method of Claim 1, wherein act (a) is performed by a controller of a memory device comprising the write-once memory array.

5. The method of Claim 1, wherein act (d) is performed by a data reading device coupled with a memory device comprising the write-once memory array.

6. The method of Claim 5, wherein the data reading device comprises a device selected from the group consisting of a digital audio player, a digital audio book, an electronic book, a digital camera, a game player, a general-purpose computer, a personal digital assistant, a portable telephone, a printer, and a projector.

7. The method of Claim 1, wherein act (d) is performed by a controller of a memory device comprising the write-once memory array.

8. A memory device comprising:

a write-once memory array storing a plurality of bits representing data; and

a controller coupled with the write-once memory array and operative to invert the plurality of bits representing the data irrespective of a number of logic one bits in the plurality of bits when the plurality of bits is read from the write-once memory array.

9. The memory device of Claim 8, wherein the controller is further operative to invert a plurality of bits representing data to be stored in the write-once memory array.

10. The memory device of Claim 8, wherein the memory device comprises a solid-state memory device.

11. The memory device of Claim 8, wherein the memory device comprises an optical memory device.

12. A method for redefining an initial, un-programmed digital state of a write-once memory array, the method comprising:

(a) providing a write-once memory array comprising a plurality of write-once memory cells, the plurality of write-once memory cells comprising an initial, un-programmed digital state that can be switched to an alternative, programmed digital state; and

(b) redefining the initial, un-programmed digital state of the plurality of write-once memory cells as the alternative, programmed digital state by storing bits in the plurality of write-once memory cells in an inverted form irrespective of a number of logic one bits in the plurality of bits.

13. The method of Claim 12, wherein the initial, un-programmed digital state comprises Logic 1, and wherein the alternative, programmed digital state comprises Logic 0.

14. The method of Claim 12, wherein the initial, un-programmed digital state comprises Logic 0, and wherein the alternative, programmed digital state comprises Logic 1.

15. The method of Claim 1 or 12, wherein the write-once memory array comprises a three-dimensional memory array.

16. The method of Claim 1 or 12, wherein the write-once memory array comprises a two-dimensional memory array.

17. The memory device of Claim 8, wherein the write-once memory array comprises a three-dimensional memory array.

18. The memory device of Claim 8, wherein the write-once memory array comprises a two-dimensional memory array.

19. The method of Claim 1, wherein the plurality of bits are inverted even when a number of logic one bits in the plurality of bits does not exceed fifty percent of a total number of bits in the plurality of bits.

20. The memory device of Claim 8, wherein the plurality of bits are inverted even when a number of logic one bits in the plurality of bits does not exceed fifty percent of a total number of bits in the plurality of bits.

21. The method of Claim 12, wherein the controller is operative to invert the plurality of bits even when a number of logic one bits in the plurality of bits does not exceed fifty percent of a total number of bits in the plurality of bits.

X. Evidence Appendix

None.

XI. Related Proceedings Appendix

None.